Claims

1. An amplifier circuit configured for use within high-speed applications, said amplifier circuit comprising:

a composite amplifier having a feedback element and a pair of input terminals for receiving an input voltage, and an output terminal configured to provide an output voltage; and

an overload recovery circuit configured for facilitating a faster overload recovery of said composite amplifier when said output voltage reaches an overload condition, said overload recovery circuit comprising:

a bypass device coupled in parallel with said feedback element, said bypass device configured to provide a path for additional current to flow through during said overload condition; and

a stabilization circuit configured for stabilizing said composite amplifier during said overload condition to prevent oscillation.

2. The amplifier circuit according to claim 1, wherein said bypass device comprises a transistor device having an input terminal coupled to said output terminal of said composite amplifier, and an output terminal coupled to an inverting input terminal of said composite amplifier.

3. The amplifier circuit according to claim 2, wherein said bypass device further comprises a control terminal coupled to an threshold comparison control signal configured to facilitate detection of said overload condition to turn on said bypass device when said overload condition is reached.

4. The amplifier circuit according to claim 3, wherein said threshold comparison control signal is generated by a bias circuit comprising a current source

coupled to a pair of diode-connected transistor devices, and a third transistor device configured between said pair of diode-connected transistor devices.

5. The amplifier circuit according to claim 1, wherein said stabilization circuit is configured to modify feedback to said pair of input terminals.

6. The amplifier circuit according to claim 5, wherein said stabilization circuit comprises:

a clamp sensing element configured to sense when said bypass device is providing said path for current flow; and

a stabilization network configured to modify feedback to said pair of input terminals of said composite amplifier.

7. The amplifier circuit according to claim 6, wherein said clamp sensing element comprises a transistor device having an input terminal coupled to said output terminal of said composite amplifier, and an output terminal coupled to said stabilization network.

8. The amplifier circuit according to claim 7, wherein said clamp sensing element further comprises a control terminal configured to receive an overload control signal configured to turn on said clamp sensing element when said overload condition is reached.

9. The amplifier circuit according to claim 5, wherein said stabilization circuit is suitably controlled by a control signal also configured to control operation of said bypass device.

10. The amplifier circuit according to claim 6, wherein said stabilization network comprises a diode device and a switch device.

11. The amplifier circuit according to claim 10, wherein said diode device comprises a diode-connected transistor, and said switch device comprises a

transistor having a control terminal coupled to a control terminal of said diode-connected transistor.

12. The amplifier circuit according to claim 1, wherein said composite amplifier further comprises a high-speed amplifier comprising said pair of input terminals and an auto-zero amplifier circuit having an output terminal coupled to one of said pair of input terminals of said high-speed amplifier.

13. An overload recovery circuit for facilitating a reduction in overload recovery time of an amplifier circuit, said overload recovery circuit comprising:

a bypass device configured for coupling in parallel with a feedback element of the amplifier circuit, said bypass device configured to provide a path for additional current to flow through during an overload condition instead of flowing through the feedback element; and

a stabilization circuit configured for stabilizing said amplifier circuit during said overload condition to prevent oscillation.

14. The overload recovery circuit according to claim 13, wherein said bypass device comprises a transistor device having an input terminal configured for coupling to an output terminal of the amplifier circuit, an output terminal configured for coupling to an inverting input terminal of the amplifier circuit, and a control terminal configured to receive an overload control signal for turning on said bypass device when said overload condition is reached.

15. The overload recovery circuit according to claim 14, wherein said overload control signal is generated by a bias circuit comprising a current source coupled to a pair of diode-connected transistor devices, and a third transistor device configured between said pair of diode-connected transistor devices.

16. The overload recovery circuit according to claim 13, wherein said stabilization circuit is configured to modify feedback to a pair of input terminals of said amplifier circuit.

17. The overload recovery circuit according to claim 16, wherein said stabilization circuit comprises:

a clamp sensing element configured to sense when said bypass device is providing said path for current flow; and

a stabilization network configured to modify the feedback to the pair of input terminals of the amplifier circuit.

18. The overload recovery circuit according to claim 17, wherein said clamp sensing element comprises a transistor device having an input terminal coupled to said output terminal of said composite amplifier, and an output terminal coupled to said stabilization network, and a control terminal configured to receive an overload control signal for turning on said clamp sensing element when said overload condition is reached.

19. The overload recovery circuit according to claim 16, wherein said stabilization circuit is suitably controlled by a control signal also configured to control operation of said bypass device.

20. The overload recovery circuit according to claim 17, wherein said stabilization network comprises a diode-connected transistor, and a switch transistor having a control terminal coupled to a control terminal of said diode-connected transistor, said transistor switch configured to modify feedback to the pair of input terminals of the amplifier circuit.

21. A method for reducing overload recovery time in an amplifier circuit, said method comprising the steps of:

sensing when an overload condition exists at an output terminal of said amplifier circuit;

providing through a bypass device a path for additional current to flow through during said overload condition; and

stabilizing said amplifier circuit during said overload condition.

22. The method according to claim 21, wherein said sensing step comprises providing a control signal representative of said overload condition to a control terminal of said bypass device such that said bypass turns on when said overload condition occurs.

23. The method according to claim 21, wherein said step of providing said path through said bypass device comprises providing said path in parallel to a feedback resistor of said amplifier circuit.

24. The method according to claim 21, wherein said step of stabilizing said amplifier circuit during said overload condition comprises modifying feedback to input terminals of the amplifier circuit.

25. The method according to claim 24, wherein said step of stabilizing said amplifier circuit comprises sensing of said overload condition, and modifying feedback to the input terminals of the amplifier circuit.

26. The method according to claim 25, wherein said step of sensing of said overload condition comprises the same process as the step of sensing when an overload condition exists at an output terminal of said amplifier circuit.

27. The method according to claim 25, wherein said step of modifying feedback to the input terminals of said amplifier circuit comprises providing a resistance between the input terminals of said amplifier circuit.

28. A transimpedance amplifier circuit configured for reduced overload recovery time, said transimpedance amplifier circuit comprising:

a high-speed amplifier having an inverting input terminal and a non-inverting input terminal configured for receiving an input signal, an output terminal configured to provide an output voltage, and a feedback element coupled between said inverting input terminal and said output terminal, said inverting input terminal configured to provide a negative input terminal for said transimpedance amplifier circuit;

an auto-zero amplifier having an inverting input terminal coupled through at least one resistor to said inverting input terminal of said composite amplifier, a non-inverting input terminal configured to provide a positive input terminal for said transimpedance amplifier circuit, and an output terminal coupled to said non-inverting input terminal of said high-speed amplifier, said high-speed amplifier and said auto-zero amplifier configured to provide a composite amplifier; and

an overload recovery circuit configured for facilitating a faster overload recovery time in said composite amplifier when said output voltage reaches an overload condition, said overload recovery circuit comprising:

a bypass device coupled in parallel with said feedback element, said bypass device configured to provide a path for additional current to flow through during said overload condition; and

a stabilization circuit configured to stabilize said composite amplifier to prevent oscillation.

29. The transimpedance amplifier according to claim 28, wherein said stabilization circuit comprises:

a clamp sensing element configured to sense when said bypass device is providing said path for current flow; and

a stabilization network configured to modify feedback to said negative input terminal and said positive input terminal of said transimpedance amplifier circuit.